16,384 X 4 Organization Single +5-V Supply (10% Tolerance)

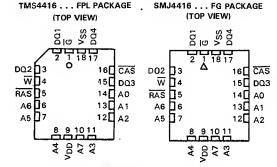
Performance Ranges:

				•	
	ACCESS	ACCESS	READ	READ-	
	TIME	TIME	OR	MODIFY-	
	ROW	COLUMN	WRITE	WRITE	
	ADDRESS	ADDRESS	CYCLE	CYCLE	
	(MAX)	(MAX)	(MIN)	(MIN)	
4416-12	120 ns	70 ns	230 ns	320 ns	
4416-15	150 ns	80 ns	260, ns	330 ns	
4416-20	200 ns	120 ns	330 ns	440 ns	

TMS4416 . . . NL PACKAGE SMJ4416 . . . JD PACKAGE (TOP VIEW)

G		U ₁₈] V _{SS}
DQ1	□ 2	17	DQ4
DQ2	□3	16	CAS
\overline{w}	4	15	DQ3
RAS	□ 5	14	A0
A6	□6	13] A1
A5	□7	12	A2
A4	□8	11	A3
V_{DD}	□ 9	10	A7

- Available Temperature Ranges*:
 - S... 55 °C to 100 °C
 - E... 40°C to 85°C
 - L . . . 0°C to 70°C
- Long Refresh Period . . . 4 milliseconds
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Early Write or G to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Low Power Dissipation
 - Operating . . . 200 mW (TYP)
 - Standby . . . 17.5 mW (TYP)
- New SMOS (Scaled-MOS) N-Channel Technology



PIN NOMENCLATURE						
A0-A7	Address Inputs					
CAS Column Address Strobe						
DQ1-DQ4	Deta in/Data Out					
G	Output Enable					
RAS	Row Address Strobe					
∨ o D	+5-V Supply					
V _{SS}	Ground '					
W	Write Enable					

description

The '4416 is a high-speed, 65,536-bit, dynamic, random-access memory, organized as 16,384 words of 4 bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The '4416 features RAS access times to 120 ns maximum. Power dissipation is 200 mW typical operating, 17.5 mW typical standby.

New SMOS technology permits operation from a single + 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. In peaks have been reduced to 60 mA typical, and a -1-V input voltage undershoot can be tolerated, minimizing system noise considerations. Input clamp diodes are used to ease system design.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with RAS in order to retain data. CAS can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All address lines and data-in are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

M temperature range (-55°C to 125°C) to be available in future.

The TMS4416 is offered in 18-pin plastic dual-in line and 18-pin plastic chip carrier packages. It is guaranteed for operation from 0°C to 70°C. The SMJ4416 is offered in 18-pin ceramic side-braze dual-in-line and 18-pin ceramic chip carrier packages. It is available in -55°C to 100°C and -40°C to 85°C temperature ranges. Dual-in-line packages are designed for insertion in mounting-hole rows on 300-mil (7,62 mm) centers.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe (RAS). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe (CAS). All addresses must be stable on or before the falling edges of RAS and CAS. RAS is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. CAS is used as a chip select activating the column decoder and the input and output buffers.

write enable (W)

The read or write mode is selected through the write enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When \overline{W} goes low prior to \overline{CAS} , data-out will remain in the high-impedance state allowing a write cycle with \overline{G} grounded.

data-in (DQ1 through DQ4)

Datá is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edga of $\overline{\text{CAS}}$ or $\overline{\text{W}}$ strobes data into the on-chip data latchas. Thasa latches can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{\text{W}}$ is brought low prior to $\overline{\text{CAS}}$ and the data is strobed in by $\overline{\text{CAS}}$ with satup and hold timas referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{\text{CAS}}$ will alraady ba low, thus the data will be strobed in by $\overline{\text{W}}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{\text{G}}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data-out (DQ1 through DQ4)

Tha three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series $\underline{54}/74$ TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until CAS is brought low. In a read cycle the output goes active after the access time interval $t_a(C)$ that begins with the negative transition of \overline{CAS} as long as $t_a(R)$ and $t_a(E)$ are satisified. The output becomes valid after the access time has elapsed and remains valid while \overline{CAS} and \overline{G} are low. \overline{CAS} or \overline{G} going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing \overline{G} high prior to applying data, thus satisfying t_{GHD} .

output enable (G)

The \overline{G} controls the impedance of the output buffers. When \overline{G} is high, the buffers will remain in the high impedance state. Bringing \overline{G} low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both \overline{RAS} and \overline{CAS} to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will reamin in the low impedance state until \overline{G} or \overline{CAS} is brought high.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless \overline{CAS} is applied, the \overline{RAS} -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power.

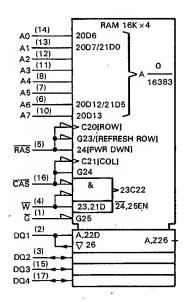
page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single RAM, the row address and \overline{RAS} are applied to multiple $16K \times 4$ RAMs. \overline{CAS} is then decoded to select the proper RAM.

power-up

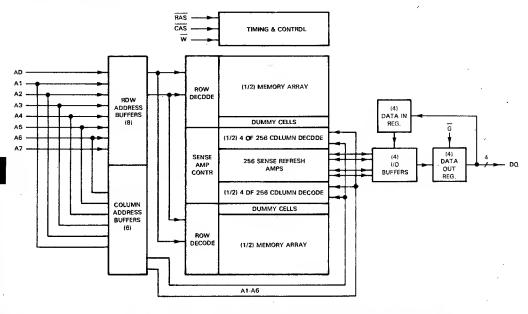
After power-up, the power supply must remain at its steady-state value for 1 ms. In addition, the \overline{RAS} input must remain high for 100 μ s immediately prior to initialization. Initialization consists of performing eight \overline{RAS} cycles before proper device operation is achieved.

logic symbol†



[†]This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See axplanation on page 10-1.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage on any pin except VDD and data out (see Note 1)	1.5 V to 10 V
Voltage on Vpp supply and data out with respect to Vss	1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range: TMS'	0°C to 70°C
Operating case temperature range: SMJ' - S version	55°C to 100°C
- E version	40°C to 85°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "Absolute Meximum Ratings" mey cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-meximum-rated conditions for extended periods may effect device reliability.

NOTE 1: All voltega values in this data sheet are with respect to VSS.

recommended operating conditions

			TMS441	16	UNIT
	PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, VDD		4.5	5	5.5	V
Supply voltage, VSS			0		V
High-level input voltage, VIH	V _{DD} = 4.5 V	2.4		4.8] _v
	V _{DD} = 5.5 V	2.4		5.8	·
Low-level input voltage, VIL (see Not		. V _{IK}		0.8	V
Deprating free-air temperature, TA		0		70	°C

NOTE 2: The algebraic convention, where the more negetive (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

			TMS4416-12			UNIT
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNII
VIK	Input clamp voltage	l₁ = −15 mA, see Figure 1			-1.2	٧
VDH	High-level output voltage	I _{OH} = -2 mA	2.4			V
VOL	Low-level output voltage	I _{OL} = 4.2 mA			0.4	V
11	Input current (leakege)	$V_I = 0 \text{ V to } 5.8 \text{ V},$ $V_{DD} = 5 \text{ V},$ All other pins = 0 V	,		±10	μΑ
lo	Output current (leakege)	$V_O = 0.4 \text{ V to } 5.5 \text{ V},$ $V_{DD} = 5 \text{ V}, \overline{\text{CAS}} \text{ high}$			±10	μΑ
I _{DD1}	Averege opereting current during read or write cycle	At t _C = minimum cycle			54	mA
I _{DD2} ‡	Standby current	After 1 memory cycle, RAS end CAS high		3.5	· 5	mA
IDD3	Averege refresh current	t _C = minimum cycle, RAS cycling, CAS high			46	mA
[†] D D 4	Average page-mode	t _{c(P)} = minimum cycle, RAS low, CAS cycling			46	mA

 $^{^{\}dagger}$ All typical values are at $T_A = 25\,^{\circ}$ C and nominal supply voltages.

 $^{^{\}ddagger}V_{IL} \ge -0.6 \text{ V on all inputs.}$

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

			TN	TMS4416-15		TMS4416-20			
	PARAMETER	TEST CONDITIONS	MIN TYPT MAX		MIN TYP [†] MAX		MAX	UNIT	
VIK	Input clamp voltage	I _I = -15 mA, see Figure 1			· - 1.2			-1.2	٧
VOH	High-level output voltage	. I _{DH} = -2 mA	2.4			2.4			٧
VOL	Low-level output voltage	I _{DL} = 4.2 mA			0.4			0.4	٧
l ₁	Input current (leakage)	$V_{\parallel} = 0 \text{ V to } 5.8 \text{ V},$ $V_{DD} = 5 \text{ V},$ All other pins = 0 V			± 10			± 10	μΑ
lo .	Dutput current (leakage)	$V_D = 0.4 \text{ V to } 5.5 \text{ V},$ $V_{DD} = 5 \text{ V}, \overline{\text{CAS}} \text{ high}$			± 10			±10	. μА
I _{DD1}	Average operating current during read or write cycle	At t _C = minimum cycle		40	48		35	42	mA
l _{DD2} ‡	Standby current	After 1 memory cycle, RAS and CAS high		3.5	5		3.5	5	mA
IDD3	Average rafresh currant	t _c = minimum cycle, RAS cycling, CAS high		25	. 40		21	34	mA
I _{DD4}	Average page-moda current	t _{c(P)} = minimum cycle, RAS low, CAS cycling		25	40		21	34	mA

 $^{^{\}dagger}\text{All typical values are at T}_{\text{A}}~=~25\,^{\text{o}}\text{C}$ and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

	PARAMETER	TMS4416	
•	PARAMETER	TYP [†] MAX	UNIT
C _{i(A)}	Input capacitance, address inputs	5 7	рF
Ci(RC)	Input capacitance, strobe inputs	8 10	pF
	Input capacitance, write enable input	8 10	. pF
C _{i(W)}	Input/output capacitance, data ports	8 10	pF

 $^{^{\}dagger}\text{All}$ typical values are at TA =25 °C and nominal supply voltages.

 $^{^{\}ddagger}V_{IL} \ge -0.6 \text{ V on all inputs.}$

TMS4416 16,384-WORD BY 4-BIT DYNAMIC RAM

switching characteristics over recommended supply voltage range and operating free-air temperature range

			ALT.	TMS4416-12		UNIT
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT
ta(C)	Access time from CAS	C _L = 100 pF, Load = 2 Series 74 TTL gates	^t CAC		70	ns
ta(R)	Access time from RAS	t _{RLCL} = MAX, C _L = 100 pF Load = 2 Series 74 TTL gates	tRAC		120	ns
t _a (G)	Access time after G low	C _L = 100 pF, Load = 2 Series 74 TTL gates			30	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	[†] OFF	0	30	ns
t _{dis} (G)	Output disable time after G high	Ct = 100 pF, Load = 2 Series 74 TTL gates		0	30	ns

			ALT.	TMS4416-15		TMS4416-20		UNIT	
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	MIN	MAX	ONII	
	Access time from CAS	C _L = 100 pF,	tCAC		80		120	ns	
ta(C)	Access time from CAS	Load = 2 Series 74 TTL gatas	CAC		00		120	110	
		t _{RLCL} = MAX,							
ta(R)	Access time from RAS	$C_L = 100 \text{ pF}$	tRAC	1	150	ŀ	200	ns	
		Load = 2 Series 74 TTL gates							
	Accass time after G low	C _L = 100 pF,			40	i	50	ns	
^t a(G)	Accass time after G low	Load = 2 Series 74 TTL gates							
	Car distribution of the CAC high	$C_{L} = 100 \text{ pF},$	torr	0	30	0	40	ns	
^t dis(CH)	Output disable time after CAS high	Load = 2 Series 74 TTL gatas	tOFF	L ů				110,	
	Output disabla time	$C_{L} = 100 \text{ pF},$		1 0	30	0	40	ns	
tdis(G)	after G high	Load = 2 Saries 74 TTL gates		L	50			1.0	

timing requirements over recommended supply voltage range and operating free-air temperature range

	DADANETED	ALT.	TMS	4416-12	UNIT
	PARAMETER	SYMBOL	MIN	MAX	UNIT
t _C (P)	Page mode cycle time	t _P C	120		ns
tc(rd) ·	Read cycle time*	^t RC	230		ns
t _c (W)	Write cycle time	twc	230		ns
t _{c(rdW)}	Read-write/read-modify-write cycle time	tRWC	320		ns
tw(CH)	Pulse width, CAS high (precharge time)**	[†] CP	40	***	ns
tw(CL)	Pulse width, CAS low f	†CAS	70	10,000	ns
tw(RH)	Pulse width RAS high (precharge time)	t _{RP}	80		ns
tw(RL)	Pulse width, RAS low [‡]	tRAS	120	10,000	ns
tw(W)	Write pulse width	twp	30		ns
tt	Transition times (rise and fall) for RAS and CAS	, tŢ	3	50	ns
tsu(CA)	Column address setup time	tASC	0		ns
t _{su(RA)}	Row address setup time	†ASR	0		ns
t _{su(D)}	Data setup time	tps	0		ns
tsu(rd)	Read command setup time	†RCS	0		ns
t _{su(WCH)}	Write command setup time before CAS high	tCWL	50		ns
t _{su} (WRH)	Write command setup time before RAS high	t _{RWL}	50		ns
th(CLCA)	Column address hold time after CAS low	tCAH	35		ns
th(RA)	Row address hold time	tRAH	15		na
th(RLCA)	Column address hold time after RAS low	tAR	85		ns
th(CLD)	Data hold time after CAS low	t _{DH}	40.		ns
th(RLD)	Data hold time after RAS low	tDHR	100		ns
th(WLD)	Data hold time after W low	t _{DH}	30		ns
th(RHrd)	Read command hold time after RAS high	trr	10		na
th(CHrd)	Read command hold time after CAS high	^t RCH	0		ns
th(CLW)	Write command hold time after CAS low	tWCH	40		ns
th(RLW)	Write command hold time after RAS low	twcr	100		ns
^t RLCH	Delay tima, RAS low to CAS high	tcsH	150		ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0		ns
[†] CLRH	Delay time, CAS low to RAS high	trsh	80		ns
	Delay time, CAS low to W low				
tCLWL	(read, modify-write-cycle only) * * *	tCMD	120		ns
	Delay time, RAS low to CAS low		1		
^t RLCL	(maximum value specified only to guarantee access time)	, tRCD	20	, 50	ns
	Delay time, RAS low to W low		430		
[†] RLWL	(read, modify-write-cycle only)***	t _{RWD}	170		ns
†WLCL	Delay time, W low to CAS low (early write cycle)	twcs	-5		ns
tGHD	Delay time, G high before data applied at DQ	7,75	30		ns
t _{rf}	Refresh time interval	†REF	1	4	ms

^{*} Note: All cycle times assume t_t = 5 ns.

^{**} Page mode only.

^{***}Necessary to insure G has disabled the output buffers prior to applying data to the device.

[†]In a read-modify-write cycle, t_{CLWL} and t_{su(WCH)} must be observed. Depending on the user's transition times, this may require additional CAS low time t_{W(CL)}.
†In a read-modify-write cycle, t_{RLWL} and t_{su(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time t_{w(RL)}.

timing requirements over recommended supply voltage range and operating free-air temperature range

Le(P) Page mode cycle time Le(P) Page mode cycle time Le(Id) Read cycle time Le(Id) Re			ALT.	TMS4416-15	TMS4416-20	UNIT
Table Tabl		PARAMETER .	SYMBOL	MIN MAX	MIN MAX	CIVIT
Vector Read cycle time* IRC 2660 330 Vec(W) Write cycle time IWC 260 330 Vec(CH) Write cycle time ItQC 260 330 Leg(CH) Pulse width, CAS high (precharge time)** ItQP 50 80 Lw(CL) Pulse width, CAS low* ItQAS 80 10,000 120 10,000 Lw(RH) Pulse width, RAS low* ItRAS 150 10,000 200 10,000 Lw(RH) Pulse width, RAS low* ItRAS 150 10,000 200 10,000 Lw(WH) Write pulse width ItWP 40 50 Lw(WI) Write pulse width ItWP 40 50 Lw(WI) Write pulse width ItWP 40 50 Lw(RI) Write and dress and fall for RAS and CAS 1T 3 50 3 50 3 50 Lw(RI) Write and dress setup time ItASR 0 0 0 Lau(D) Data setup time ItASR 0 0 0 Lau(D)	t _c (P)	Page mode cycle time	tPC	140	210	ns
te(W) Write cycle time tWC 260 330 Te(rdW) Read-write/read-modify-write cycle time tRWC 360 440 Te(rdW) Pulse width, CAS high (precharge time)** tcp 50 80 Lw(CL) Pulse width, CAS high (precharge time)** tcAS 80 10,000 120 10,000 Lw(RL) Pulse width, RAS high (precharge time) tpP 100 120 Lw(RL) Pulse width, RAS low * trASS 150 10,000 200 10,000 Lw(RL) Pulse width, RAS low * trASS 150 0,000 200 10,000 Lw(RL) Write pulse width trASS 0 0 Lw(WW) Write pulse width trASS 0 0 Lw(CA) Column address setup time trASS 0 0 Lsu(CA) Column address setup time trASS 0 0 Lsu(D) Data setup time trASS 0 0 Lsu(DA) Read command setup time before CAS high trAWL 60 80 Lsu(WH)		Read cycle time*	tRC	260	330	ns
		Write cycle time	tWC	260	330	ns
tw(CH) Pulse width, CAS high (precharge time)** t_CP 50 80 tw(CL) Pulse width, CAS low** tCAS 80 10,000 120 10,000 tw(RH) Pulse width RAS high (precharge time) tRP 100 120 tw(RH) Pulse width RAS high (precharge time) tRP 100 120 tw(RH) Pulse width, RAS low** tRAS 150 10,000 200 10,000 tw(RH) Write pulse width tWP 40 50 tw(W) Write pulse width tWP 40 50 tw(W) Write pulse width tWP 40 50 tw(W) Write pulse width tWP 40 50 su(RA) Row address setup time tASC 0 0 su(WH) Write command setup time before RAS high tCWL		Read-write/read-modify-write cycle time	tRWC	360	440	ns
t_w(CL) Pulse width, CAS low¹ t_CAS 80 10,000 120 10,000 t_w(RH) Pulse width RAS high (precharge time) t_RP 100 120 10,000 t_w(RL) Pulse width, RAS low² t_RAS 150 10,000 200 10,000 t_w(W) Write pulse width t_WP 40 50 t_w(CLA) Column address setup time t_ASC 0 0 t_w(RA) Road accommand setup time t_RCS 0 0 0 t_w(CLA) Write command setup time before RAS high t_RWL 60 80 0 t_w(WH) Write command setup time before RAS high t_RWL 60 80 0 t_w(CLA) Write command setup time before RAS high t_RWL 10 80 <t< td=""><td></td><td>Pulse width, CAS high (precharge time)**</td><td>t_{CP}</td><td>50</td><td>80</td><td>ns</td></t<>		Pulse width, CAS high (precharge time)**	t _{CP}	50	80	ns
Fw(RH) Pulse width RAS high (precharge time) tRP 100 120 tw(RL) Pulse width, RAS low* tRAS 150 10,000 200 10,000 tw(W) Write pulse width twp 40 50 10,000 tw(W) Write pulse width twp 40 50 10 tw(W) Transition times (rise and fall) for RAS and CAS tr 3 50 3 50 tw(CA) Column address setup time tASC 0 0 0 0 tsu(RA) Row address setup time tASR 0 0 0 0 tsu(BC) Data setup time treas treas 0 0 0 tsu(WCH) Write command setup time before CAS high tcWL 60 80 0 tsu(WCH) Write command setup time before CAS high trWL 60 80 0 tsu(WCH) Write command setup time before CAS high transition transition transition transition transition tran			tCAS	80 10,000	120 10,000	ns
tw(RL) Pulse width, RAS low ‡ tRAS 150 10,000 200 10,000 tw(RW) Write pulse width twp 40 50 tw(W) Write pulse width twp 40 50 tw(CA) Column address setup time tASC 0 0 tsu(CA) Row address setup time tASR 0 0 tsu(D) Data setup time tDS 0 0 tsu(D) Data setup time tRCS 0 0 tsu(WCH) Write command setup time before CAS high tCWL 60 80 tsu(WCH) Write command setup time before CAS high tRWL 60 80 tsu(WCH) Write command setup time before RAS high tRWL 60 80 tsu(WCH) Write command setup time before RAS high tRWL 60 80 th(CLCA) Column address hold time after CAS low tCAH 40 50 th(RLCA) Column address hold time after RAS low tAR 110 130 th(RLCA) Data hold t			tRP	100	120	ns
t_w(W) Write pulse width typ 40 50 t_t Transition times (rise and fall) for RAS and CAS t_T 3 50 3 50 tsu(CA) Column address setup time tASR 0 0 0 tsu(A) Row address setup time tASR 0 0 0 tsu(D) Data setup time tDS 0 0 0 tsu(D) Post a setup time tRCS 0 0 0 tsu(WCH) Write command setup time before CAS high tCWL 60 80 80 tsu(WCH) Write command setup time before RAS high tRWL 60 80 80 tsu(WCH) Write command setup time before RAS high tRWL 60 80 80 th(CLCA) Column address hold time after CAS low tCAH 40 50 80 th(RLCA) Column address hold time after RAS low tDH 60 80 80 th(RLCA) Data hold time after CAS low tDH 60 80		Pulse width RAS low‡	tRAS	150 10,000	200 10,000	ns
tt Transition times (rise and fall) for RAS and CAS tT 3 50 3 50 tsu(CA) Column address setup time tASC 0 0 0 tsu(RA) Row address setup time tASR 0 0 0 tsu(D) Data setup time tDS 0 0 0 tsu(WCH) Write command setup time before CAS high tCWL 60 80 tsu(WCH) Write command setup time before RAS high tRWL 60 80 tsu(WCH) Write command setup time before RAS high tRWL 60 80 tsu(WCH) Write command setup time before RAS high tRWL 60 80 tsu(WCH) Write command setup time before RAS high tRWL 60 80 th(CLCA) Column address hold time after CAS low tCAH 40 50 th(RLCA) Column address hold time after RAS low tAR 110 130 th(RLCA) Column address hold time after RAS low tDH 60 80 th(RLDD) <			tWP	40	50	ns
tsu(CA) Column address setup time tASC 0 0 tsu(RA) Row address setup time tASR 0 0 tsu(D) Data setup time tDS 0 0 tsu(MCH) Write command setup time before CAS high tCWL 60 80 tsu(WRH) Writa command setup time before CAS high tRWL 60 80 tsu(WRH) Writa command setup time before CAS high tRWL 60 80 tsu(WRH) Writa command setup time before CAS high tRWL 60 80 tsu(WRH) Writa command setup time before CAS high tRWL 60 80 th(CLCA) Column address hold time after CAS low tCAH 40 50 50 th(RLD) Data hold time after CAS low tDH 60 80 60 80 th(RLD) Data hold time after CAS low tDH 40 50 60 80 th(RH)D Data hold time after CAS low tDH 40 50 60 60 60 60		Transition times (rise and fall) for RAS and CAS	tτ	3 50	3 50	ns
tsu(RA) Row address setup time tASR 0 0 tsu(D) Data setup time tDS 0 0 tsu(rd) Read command setup time tRCS 0 0 0 tsu(WCH) Write command setup time before CAS high tCWL 60 80 tsu(WRH) Write command setup tima before RAS high tRWL 60 80 tsu(WRH) Write command setup tima before RAS high tRWL 60 80 tsu(WRH) Write command setup tima before RAS high tRWL 60 80 th(CLCA) Column address hold time after CAS low tCAH 40 50 th(RA) Row address hold time after CAS low tAR 110 130 th(CLD) Data hold time after CAS low tDH 60 80 th(RLD) Data hold time after RAS low tDH 40 50 th(RHD) Data hold time after RAS high tRRH 10 10 th(CHR) Read command hold time after CAS low tWCH 60 80			tASC	0	0	ns
tsu(D) Data setup time tps 0 0 tsu(rd) Read command setup time tRCS 0 0 tsu(WCH) Write command setup time before CAS high tCWL 60 80 tsu(WRH) Writa command setup time before RAS high tRWL 60 80 th(CLCA) Column address hold time after CAS low tCAH 40 50 th(RAL) Row address hold time after RAS low tAR 110 130 th(RLCA) Column address hold time after RAS low tAR 110 130 th(RLCA) Column address hold time after RAS low tDH 60 80 th(RLCA) Column address hold time after RAS low tDH 60 80 th(RLD) Data hold time after RAS low tDH 60 80 th(RLD) Data hold time after RAS low tDH 40 50 th(RLD) Data hold time after RAS high tRRH 10 10 th(RHd) Raad command hold time after RAS high tRCH 0 0		Row address setup time	tASR	0	0	ns
tsu(rd) Read command setup time tRCS 0 0 tsu(WCH) Write command setup time before CAS high tCWL 60 80 tsu(WRH) Writa command setup time before RAS high tRWL 60 80 tsu(WRH) Writa command setup time before RAS high tRWL 60 80 th(CLCA) Column address hold time after RAS low tCAH 40 50 th(RA) Row address hold time tRAH 20 25 th(RLD) Data hold time after RAS low tDH 60 80 th(CLD) Data hold time after CAS low tDH 60 80 th(RLD) Data hold time after RAS low tDH 40 50 th(RLD) Data hold time after RAS high tRRH 10 10 th(RHn) Raad command hold time after RAS high tRRH 10 10 th(CHrd) Raad command hold time after CAS low tWCH 60 80 th(CHrd) Raad command hold time after RAS low tWCH 60 80		Data setup time	tDS	0	0	ns
tsu(WCH) Write command setup time before CAS high tCWL 60 80 tsu(WRH) Writa command setup time before RAS high tRWL 60 80 th(CLCA) Column address hold time after CAS low tCAH 40 50 th(RLA) Row address hold time after CAS low tRAH 20 25 th(RLA) Column address hold time after RAS low tAR 110 130 th(RLD) Data hold time after CAS low tDH 60 80 th(RLD) Data hold time after RAS low tDHR 130 160 th(RLD) Data hold time after RAS low tDH 40 50 th(RLD) Data hold time after RAS low tDH 40 50 th(RHrd) Raad command hold time after RAS high tRRH 10 10 th(CHrd) Raad command hold time after CAS low tWCH 60 80 th(CHrd) Raad command hold time after CAS low tWCH 60 80 th(CHrd) Raad command hold time after CAS low tWCH 60			^t RCS	0	0	ns
tsu(WRH) Writa command setup tima before RAS high tRWL 60 80 th(CLCA) Column address hold time after CAS low tCAH 40 50 th(RA) Row address hold time tRAH 20 25 th(RLCA) Column address hold time after RAS low tAR 110 130 th(RLCA) Column address hold time after RAS low tAR 110 130 th(RLD) Data hold tima after CAS low tDH 60 80 th(RLD) Data hold tima after RAS low tDHR 130 160 th(RLD) Data hold tima after RAS high tRRH 10 10 th(RHD) Raad command hold tima after RAS high tRRH 10 10 th(CHrd) Raad command hold tima after CAS low tWCH 60 80 th(CHW) Writa command hold tima after CAS low tWCH 60 80 th(RLW) Writa command hold tima after RAS low tWCR 130 160 tRLCH Delay time, RAS low to CAS high tCSH 150 20 </td <td></td> <td></td> <td>tCWL</td> <td>60</td> <td>80</td> <td>ns</td>			tCWL	60	80	ns
th(CLCA) Column address hold time after CAS low t_CAH 40 50 th(RA) Row address hold time t_RAH 20 25 th(RLCA) Column address hold time after RAS low t_AR 110 130 th(CLD) Data hold time after CAS low tDH 60 80 th(RLD) Data hold time after RAS low tDHR 130 160 th(RLD) Data hold time after RAS low tDHR 130 160 th(RLD) Data hold time after RAS low tDHR 10 50 th(RLD) Data hold time after RAS low tDHR 10 10 th(RLM) Raad command hold tima after RAS high tRRH 10 10 th(CLW) Write command hold time after CAS low tWCR 130 160 th(RLW) Write command hold time after RAS low tWCR 130 160 tRLCH Delay time, RAS low to CAS high tCSH 150 200 tCHRL Delay time, CAS low to RAS high tRSH 80 120			tRWL	60	80	ns
th(RA) Row address hold time tRAH 20 25 th(RLCA) Column address hold time after RAS low tAR 110 130 th(CLD) Data hold time after CAS low tDH 60 80 th(RLD) Data hold time after RAS low tDHR 130 160 th(RLD) Data hold time after RAS low tDH 40 50 th(RHM) Raad command hold time after RAS high tRRH 10 10 th(RHM) Raad command hold time after CAS high tRCH 0 0 th(CLW) Write command hold time after CAS low tWCH 60 80 th(RLW) Write command hold time after RAS low tWCR 130 160 th(RLW) Write command hold time after RAS low tWCR 130 160 th(RLW) Write command hold time after RAS low tWCR 130 160 th(RLW) Write command hold time after RAS low tWCR 130 160 th(RLW) Write command hold time after RAS low tCSH 150 200			^t CAH	40	50	ns
th(RLCA) Column address hold time after RAS low tAR 110 130 th(CLD) Data hold time after CAS low tDH 60 80 th(RLD) Data hold time after RAS low tDHR 130 160 th(RLD) Data hold time after RAS low tDH 40 50 th(RHMD) Raad command hold time after RAS high tRRH 10 10 th(RHM) Raad command hold time after CAS high tRCH 0 0 th(CLW) Write command hold time after CAS low tWCH 60 80 th(RLW) Write command hold time after RAS low tWCR 130 160 th(RLW) Write command hold time after RAS low tWCR 130 160 th(RLW) Write command hold time after RAS low tWCR 130 160 th(RLW) Write command hold time after RAS low tWCR 130 160 th(RLW) Write command hold time after RAS low tWCR 130 160 th(RLW) Delay time, RAS low to CAS high tCSH 150		The state of the s	tRAH	20	25	ns
th(CLD) Data hold tima after CAS low tDH 60 80 th(RLD) Data hold time after RAS low tDHR 130 160 th(RLD) Data hold time after RAS low tDHR 130 160 th(WLD) Data hold time after RAS high tDH 40 50 th(RHrd) Raad command hold tima after RAS high tRRH 10 10 th(CHrd) Raad command hold time after CAS high tRCH 0 0 th(CLW) Writa command hold time after CAS low tWCH 60 80 th(CLW) Writa command hold time after RAS low tWCR 130 160 th(RLW) Writa command hold time after RAS low tWCR 130 160 th(LHW) Writa command hold time after RAS low tWCR 130 160 th(LW) Writa command hold time after RAS low tWCR 130 160 th(LW) Delay time, RAS low to CAS high tCSH 150 200 tCHRL Delay time, CAS low to Work (read, modify-write-cycle only)**** tRCD		Column address hold time after RAS low	tAR	110	130	ns
th(RLD) Data hold time after RAS low tDHR 130 160 th(RLD) Data hold tima after RAS low tDH 40 50 th(RHrd) Raad command hold tima after RAS high tRRH 10 10 th(CHrd) Raad command hold tima after CAS high tRRH 0 0 th(CHrd) Raad command hold tima after CAS low tWCH 60 80 th(CLW) Writa command hold tima after RAS low tWCR 130 160 th(RLW) Writa command hold tima after RAS low tWCR 130 160 th(RLW) Writa command hold tima after RAS low tWCR 130 160 th(RLW) Writa command hold tima after RAS low tWCR 130 160 tRLCH Delay time, RAS low to CAS high tCSH 150 200 tCHR Delay time, CAS high to RAS low tCRP 0 0 0 tCLRH Delay time, CAS low to Wow (read, modify-write-cycle only)*** tCWD 120 150 tRLCL Delay time, RAS low to Wow (maximum value specified			tDH	60	80	ns
th(WLD) Data hold tima aftar W low tpH 40 50 th(RHrd) Raad command hold tima after RAS high trRH 10 10 th(CHrd) Raad command hold tima after CAS high trRH 0 0 th(CHrd) Raad command hold tima after CAS low trRCH 0 0 th(CHW) Writa command hold tima after RAS low twCH 60 80 th(RLW) Writa command hold tima after RAS low twCH 130 160 th(RLW) Writa command hold tima after CAS low twCR 130 160 th(RLW) Writa command hold tima after CAS low twCR 130 160 tRLCH Delay time, RAS low to CAS high tcSH 150 200 tCHRL Delay time, CAS high to RAS low trRSH 80 120 tCLRH Delay time, CAS low to W low tcWD 120 150 tRLCL Delay time, RAS low to CAS low trRCD 20 70 25 80 tRLWL Delay time, RAS low to CAS low (early write cycle)			^t DHR	130	160	ns
th(RHrd) Raad command hold tima after RAS high tRRH 10 10 th(CHrd) Raad command hold tima after CAS high tRCH 0 0 th(CLW) Writa command hold time after CAS low tWCH 60 80 th(RLW) Writa command hold time after RAS low tWCR 130 160 th(RLW) Writa command hold time after RAS low tWCR 130 160 th(RLW) Writa command hold time after CAS low tWCR 130 160 th(RLW) Delay time, RAS low to CAS high tCSH 150 200 tCHRL Delay time, CAS high to RAS low tCSH 150 200 120 tCLRH Delay time, CAS low to W low tCWD 120 150 150 tCLWL Delay time, RAS low to CAS low tRCD 20 70 25 80 tRLWL Delay time, RAS low to W low tRWD 190 230 20 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 tGHD			^t DH	40	50	ns
th(CHrd) Raad command hold time after CAS high tRCH O O th(CLW) Write command hold time after CAS low tWCH 60 80 th(RLW) Write command hold time after RAS low tWCR 130 160 tRLCH Delay time, RAS low to CAS high tCSH 150 200 tCHRL Delay time, CAS high to RAS low tCRP 0 0 tCLRH Delay time, CAS low to RAS high tRSH 80 120 tCLWL Delay time, CAS low to W low (read, modify-write-cycle only)**** tCWD 120 150 tRLCL Delay time, RAS low to CAS low (maximum value specified only to guarantee access time) tRCD 20 70 25 80 tRLWL Delay time, RAS low to W low (read, modify-write-cycle only)**** tRWD 190 230 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 tGHD Delay time, G high before data applied at DQ 30 40			trrh	10	10	ns
th(CLW) Writa command hold time after CAS low tWCH 60 80 th(RLW) Writa command hold time after RAS low tWCR 130 160 tRLCH Delay time, RAS low to CAS high tCSH 150 200 tCHRL Delay time, CAS high to RAS low tCRP 0 0 tCLRH Delay time, CAS low to RAS high tRSH 80 120 tCLWL Delay time, CAS low to W low (read, modify-write-cycle only)**** tCWD 120 150 tRLCL Delay time, RAS low to CAS low (maximum value specified only to guarantee access time) tRCD 20 70 25 80 tRLWL Delay time, RAS low to W low (read, modify-write-cycle only)**** tRWD 190 230 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 tGHD Delay time, G high before data applied at DQ 30 40			tRCH	0	0	ns
th(RLW) Write command hold time after RAS low tWCR 130 160 tRLCH Delay time, RAS low to CAS high tCSH 150 200 tCHRL Delay time, CAS high to RAS low tCRP 0 0 tCLRH Delay time, CAS low to RAS high tRSH 80 120 tCLWL Delay time, CAS low to W low (read, modify-write-cycle only)*** tCWD 120 150 tRLCL Delay time, RAS low to CAS low (maximum value specified only to guarantee access time) tRCD 20 70 25 80 tRLWL Delay time, RAS low to W low (read, modify-write-cycle only)**** tRWD 190 230 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 tGHD Delay time, G high before data applied at DQ 30 40		Write command hold time after CAS low	tWCH	60	80	,ns
TRLCH Delay time, RAS low to CAS high tCSH 150 200 tCHRL Delay tima, CAS high to RAS low tCRP 0 0 tCLRH Delay time, CAS low to RAS high tRSH 80 120 tCLWL Delay time, CAS low to W low (read, modify-write-cycle only)**** tCWD 120 150 tRLCL Delay time, RAS low to CAS low (maximum value specified only to guarantee access time) (maximum value specified only to guarantee access time) tRCD 20 70 25 80 tRLWL Delay time, RAS low to W low (read, modify-write-cycle only)**** tRWD 190 230 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 tGHD Delay time, G high before data applied at DQ 30 40			twcr	130	160	ns
tCHRL Delay tima, CAS high to RAS low tCRP 0 0 tCLRH Delay time, CAS low to RAS high tRSH 80 120 tCLWL Delay tima, CAS low to W low (read, modify-write-cycle only)*** tCWD 120 150 tRLCL Delay time, RAS low to CAS low (maximum value specified only to guarantee access time) tRCD 20 70 25 80 tRLWL Delay time, RAS low to W low (read, modify-write-cycle only)*** tRWD 190 230 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 tGHD Delay time, G high before data applied at DQ 30 40			tCSH	150	200	ns
tCLRH Delay time, CAS low to RAS high tRSH 80 120 tCLWL Delay tima, CAS low to W low (read, modify-write-cycle only) *** tCWD 120 150 tRLCL Delay time, RAS low to CAS low (maximum value specified only to guarantee access time) (maximum value specified only to guarantee access time) tRCD 20 70 25 80 tRLWL Delay time, RAS low to W low (read, modify-write-cycle only) *** tRWD 190 230 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 tGHD Delay time, G high before data applied at DQ 30 - 40			tCRP .	0	0	ns
tCLWL Delay tima, CAS low to W low (read, modify-write-cycle only)*** tCWD 120 150 tRLCL Delay time, RAS low to CAS low (maximum value specified only to guarantee access time) tRCD 20 70 25 80 tRLWL Delay time, RAS low to W low (read, modify-write-cycle only)**** tRWD 190 230 230 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 -5 tGHD Delay time, G high before data applied at DQ 30 40 40			t _{RSH} ·	80	120	ns
tCLWL (read, modify-write-cycle only)*** CWD 1 CWD 1 2 2 70 25 80 tRLCL Delay time, RAS low to CAS low (maximum value specified only to guarantee access time) tRCD 20 70 25 80 tRLWL Delay time, RAS low to W low (read, modify-write-cycle only)*** tRWD 190 230 230 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 -5 tGHD Delay time, G high before data applied at DQ 30 40 40	CLITI			120	150	ns
TRLCL Delay time, RAS low to CAS low (maximum value specified only to guarantee access time) tRCD 20 70 25 80 TRLWL Delay time, RAS low to W low (read, modify-write-cycle only)*** tRWD 190 230 230 TWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 -5 TGHD Delay time, G high before data applied at DQ 30 40 40	tCLWL	(read, modify-write-cycle only) ***	1CMD	120	130	3
tRLCL (maximum value specified only to guarantee access time) tRCD 25 70 25 60 tRLWL Delay time, RAS low to W low (read, modify-write-cycle only)*** tRWD 190 230 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 tGHD Delay time, G high before data applied at DQ 30 40		Delay time, RAS low to CAS low		20 70	25 80	ns
tRLWL Delay time, RAS low to W low (read, modify-write-cycle only)*** tRWD 190 230 tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 tGHD Delay time, G high before data applied at DQ 30 -40	^t RLCL	•	TRCD	20 70	23 00	113
trick (read, modify-write-cycle only)*** trick 1 2 1 2 2 1 2 2 1 2 1 2 2 1 2 2 2 2 2 2 2 2 2 2			4	100	230	ns
tWLCL Delay time, W low to CAS low (early write cycle) tWCS -5 -5 tGHD Delay time, G high before data applied at DQ 30 40	^t RLWL		tRWD	190	. 230	113
tGHD Delay time, \overline{G} high before data applied at DQ 30 40	twi ci	Delay time, W low to CAS low (early write cycle)	twcs	-5	-5	ns
				30	. 40	ns
t _{rf} Refresh time interval			tBEE	4	· 4	ms

Note: All cycle times assume t_t = 5 ns.

^{**} Page mode only

^{***} Necessary to insure \widehat{G} has disabled the output buffers prior to applying data to the device.

[†] In a read-modify-write cycle, t_{CLWL} and t_{su(WCH)} must be observed. Depending on the user's transition times, this may require additional CAS low time t_{W(CL)}.

Fin a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional RAS low time $t_{W(RL)}$.

recommended operating conditions

				SMJ	1416			
PARAMETI	ER		S VERSI	ON	E	VERSI	ON	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, VDD		4.5	5	5.5	4.5	5	5.5	٧
Supply voltage, VSS			0			0		٧
Illah I and	V _{DD} = 4.5 V	2.4		4.8	2.4		4.8	V
High-level input voltage, VIH	V _{DD} = 5.5 V	2.4		5.8	2.4		5.8	V
Low-level input voltege, VIL (see Note	2)	VIK		0.8	VIK		0.8	٧
Operating case temperature, TC		- 55		100	-40		85	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

		TEST CONDITIONS	SN	J4416	-12	UNIT
	PARAMETER	TEST CONDITIONS		TYP [†]	MAX	UNII
VIK	Input clamp voltage	l _l ≃ −15 mA, see Figure 1			-1.2	>
Voн	High-level output voltage	I _{OH} = −2 mA	2.4			٧
VOL	Low-level output voltage	I _{OL} = 4.2 mA			0.4	٧
lų	Input current (leakege)	V _I = 0 V to 5.8 V, V _{DD} = 5 V, All other pins = 0 V			±10	. μΑ
ю	Output current (leekege)	$V_O = 0.4 \text{ V to } 5.5 \text{ V},$ $V_{DD} = 5 \text{ V}, \overline{\text{CAS}} \text{ high}$			±10	μΑ
I _{DD1}	Average opereting current during read or write cycle	At t _C = minimum cycle			54	mA
lDD2 [‡]	Standby current	After 1 memory cycle, RAS end CAS high		3.5	5	mA
lDD3	Average refresh current	t _C = minimum cycle, RAS cycling, CAS high			46	mA
I _{DD4}	Average page-mode current	t _{c(P)} = minimum cycle, RAS low, CAS cycling			46	mA

 $^{^{\}dagger} All$ typical values are at $T_{\mbox{\scriptsize C}}\,=\,25\,^{\rm o} \mbox{\scriptsize C}$ and nominal supply volteges.

 $^{^{\}ddagger}V_{1L} \ge -0.6 \text{ V on all inputs.}$

SMJ4416 16,384-WORD BY 4-BIT DYNAMIC RAM

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

			SI	SMJ4416-15		SMJ4416-20			UNIT
	PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	Input clamp voltage	$I_{\parallel} = -15 \text{ mA},$ see Figure 1			- 1.2			-1.2	٧
V _{DH}	High-level output voltage	l _{OH} = −2 mA	2.4			2.4			V
VOL	Low-level output voltage	I _{OL} = 4.2 mA			0.4			0.4	V
l _l	Input current (leakage)	$V_I = 0 V \text{ to } 5.8 V,$ $V_{DD} = 5 V,$ All other pins = 0 V			± 10			±10	μΑ
Ю	Output current (leakage)	$V_O = 0.4 \text{ V to } 5.5 \text{ V},$ $V_{DD} = 5 \text{ V}, \overline{\text{CAS}} \text{ high}$			± 10			±10	μΑ
I _{DD1}	Average operating current during read or write cycle	At t _C = minimum cycle		40	48		35	42	mA
I _{DD2} ‡	Standby current	After 1 memory cycle, RAS and CAS high		3.5	5		3.5	5	mA
IDD3	Average refresh current	t _C = minimum cycle, RAS cycling, CAS high		25	40		21	34	mA
I _{DD4}	Average page-mode current	$t_{C(P)} = minimum cycle,$ \overline{RAS} low, \overline{CAS} cycling		25	40		21	34	mA

 $^{^{\}dagger}$ All typical values are at † C = 25 °C and nominal supply voltages.

capacitance over recommended supply voltage range and operating case temperature range, f=1 MHz

PARAMETER		SMJ441 TYP [†] M	6 AX	INIT
Ci(A)	Input capacitance, address inputs	` 5	7 p	рF
Ci(RC)	Input capacitance, strobe inputs	В	10 p	ρF
C _{i(W)}	Input capacitance, write enable input	8	10 p	рF
C _{i/o}	Input/output capacitance, data ports	8	10 p	рF

 $^{^{\}dagger}\text{All typical values are at T}_{\text{C}}$ =25 °C and nominal supply voltages.

 $^{^{\}ddagger}V_{|L} \ge -0.6 \text{ V on all inputs.}$

switching characteristics over recommended supply voltage range and operating case temperature range

			ALT.	SMJ44	UNIT	
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNII
^t a(C)	Access time from CAS	C _L = 100 pF, Load = 2 Series 74 TTL gates	tCAC		70	ns
t _{a(R)}	Access time from RAS	tRLCL = MAX, CL = 100 pF Load = 2 Series 74 TTL gates	^t RAC		120	ns
t _a (G)	Access time after G low	C _L = 100 pF, Load = 2 Series 74 TTL gates			30	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	30	ns
^t dis(G)	Output disable time after G high	C _L = 100 pF, Load = 2 Series 74 TTL gates		0	30	ns

			ALT.	SMJ4416-15		SMJ4416-20		UNIT
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	MIN	MAX	ONI
t _e (C)	Access time from CAS	CL = 100 pF, Load = 2 Series 74 TTL gates	†CAC		80		120	ns
t _e (R)	Access time from RAS	t _{RLCL} = MAX, C _L = 100 pF Load = 2 Series 74 TTL gates	^t RAC		150		200	ns
t _a (G)	Access time after G low	C _L = 100 pF, Load = 2 Series 74 TTL getes			40		50	ne
t _{dis} (CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	30	0	40	ns
t _{dis(G)}	Output disable time after G high	C _L = 100 pF, Load = 2 Series 74 TTL gates		0	30	0	40	ns

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timing requirements over recommended supply voltage range and operating case temperature range

		ALT.	SMJ	SMJ4416-12		
	PARAMETER	SYMBOL	MIN	MAX	UNIT	
t _C (P)	Page mode cycle time	tPC	120		ns	
tc(rd)	Read cycle time*	tRC	230		ns	
t _c (W)	Write cycle time	twc	230		ns	
t _{c(rdW)}	Read-write/read-modify-write cycle time	tRWC	320		ns	
tw(CH)	Pulse width, CAS high (precharge time)**	t _{CP}	40		ns	
tw(CL)	Pulse width, CAS low†	tCAS	70	10,000	ns	
tw(RH)	Pulse width RAS high (precharge time)	tŔP	80		ns	
t _{w(RL)}	Pulse width, RAS low‡	tRAS	120	10,000	ns	
tw(W)	Write pulse width	tWP	30		ns	
t _t	Transition times (rise and fall) for RAS and CAS	t _T	3	50	ns	
t _{su(CA)}	Column address setup time	· tASC	0		ns	
t _{su(RA)}	Row address setup time	†ASR	0		ns	
t _{su(D)}	Data setup time	t _{DS}	0		ns	
t _{su(rd)}	Read command setup tima	tRCS	0		ns	
tsu(WCH)	Write command setup time before CAS high	tcWL	50		ns	
t _{su(WRH)}	Write command setup time before RAS high	tRWL	. 50		ns	
th(CLCA)	Column address hold time after CAS low	tCAH	35		ns	
th(RA)	Row address hold time	†RAH	15		ns	
th(RLCA)	Column address hold time after RAS low	t _{AR}	85		ns	
th(CLD)	Data hold tima after CAS low	t _{DH}	40		ns	
th(RLD)	Data hold time after RAS low	t _{DHR}	100		ns	
th(WLD)	Data hold time after W low	t _{DH}	30		ns	
th(RHrd)	Read command hold time after RAS high	t _{BBH}	10		ns	
th(CHrd)	Raad command hold tima aftar CAS high	^t RCH	0		ns	
th(CLW)	Write command hold time after CAS low	twch	40		ns	
th(RLW)	Write command hold time after RAS low	twcr	100		ns	
tRLCH	Delay time, RAS low to CAS high	tcsh	150		ns	
tCHRL	Delay time, CAS high to RAS low	†CRP	0		ns	
tCLRH	Delay tima, CAS low to RAS high	tRSH	80		ns	
CLAH	Delay tima, CAS low to W low		100			
tCLWL	(read, modify-write-cycla only)***	tCWD	120		ns	
	Delay time, RAS low to CAS low					
^t RLCL	(maximum value specified only to guarantee access time)	tRCD	20	50	ns	
	Delay time, RAS low to W low		172		Ī	
tRLWL	(read, modify-write-cycle only).* * *	t _{RW} D	170		ns	
tWLCL	Delay time, W low to CAS low (early write cycle)	- twcs	-5		ns	
	Delay time, G high before data applied at DQ		30		ns	
tGHD_	Refresh time interval	tREF		4	ms	
t _{rf}	Helicoli tilic alterval	1 1111			<u> </u>	

Note: All cycle times assume t_t = 5 ns.

^{**} Page mode only.

^{***}Necessary to insure \overline{G} has disabled the output buffers prior to applying data to the device.

[†]In a read-modify-write cycle, t_{CLWL} and t_{su(WCH)} must be observed. Depending on the user's transition times, this may require additional <u>CAS</u> low time t_{W(CL)}.
†In a read-modify-write cycle, t_{RLWL} and t_{su(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time t_{w(RL)}.

timing requirements over recommended supply voltage range and operating case temperature range

	PARAMETER	ALT.	SMJ4416-15	SMJ	4416-2D	UNIT
	PARAIVIETEN	SYMBOL	MIN MAX	MIN	MAX	UNIT
t _{c(P)}	Page mode cycle time	tPC	140	21D		ns
t _{c(rd)}	Read cycle time*	tRC	26D	330		ns
tc(W)	Write cycle time	twc	26D	330		ns
tc(rdW)	Read-write/read-modify-write cycle time	tRWC	36D	440		ns
tw(CH)	Pulse width, CAS high (precharge time)**	tCP	5D	8D		ns
tw(CL)	Pulse width, CAS low†	tCAS	` 80 10,000	12D	1D,D00	ns
tw(RH)	Pulse width RAS high (precharge time)	tRP	100	120		ns
tw(RL)	Pulse width, RAS low [‡]	tRAS	15D 1D,DDD	20D.	10,DDD	ns
t _W (W)	Write pulse width	tWP	4D	50		ns
t _t	Transition times (rise and fall) for RAS and CAS	tΤ	3 5D	3	50	ns
t _{su(CA)}	Column address setup time	tASC	D	D		ns
t _{su(RA)}	Row address setup time	[†] ASR	0	D		ns
t _{su(D)}	Data setup time	t _{DS}	0	0		ns
t _{su(rd)}	Read command setup time	†RCS	D	D		ns
t _{su(WCH)}	Write command setup time before CAS high	†CWL	60	8D		ns
tsu(WRH)	Write command setup time before RAS high	tRWL-	60	80		ns
th(CLCA)	Column address hold time after CAS low	^t CAH	40	50		ns
th(RA)	Row eddress hold time	^t RAH	20	25		ns
th(RLCA)	Column address hold time efter RAS low	t _{AR}	110	130		nş
th(CLD)	Data hold time efter CAS low	t _{DH}	60	80		ns
th(RLD)	Date hold time after RAS low	^t DHR	130	180		ns
th(WLD)	Data hold time after W low	^t DH	40	50		ns
th(RHrd)	Reed command hold time after RAS high	tRRH	10	10		ns
th(CHrd)	Read command hold time after CAS high	tRCH	0	0		ns
th(CLW)	Write commend hold time after CAS low	tWCH	60	80		ns
th(RLW)	Write commend hold time after RAS low	tWCR	130	160		, ns
^t RLCH	Deley time, RAS low to CAS high	tCSH	150	200		ns
tCHRL .	Delay time, CAS high to RAS low	tCRP	0	0		ns
^t CLRH	Delay time, CAS low to RAS high	^t RSH	80	120		ns
• • • • • • • • • • • • • • • • • • • •	Delay time, CAS low to W low	+0.410	120	150		ns
tCLWL	(read, modify-write-cycle only) ***	tCMD	120	130		113
	Delay time, RAS low to CAS low	*****	20 70	25	80	ns
^t RLCL	(maximum value specified only to guarantee access time)	tRCD	20 /0	2.5		113
******	Delay time, RAS low to W low	town	190	230		ns
tRLWL	(read, modify-write-cycle only)***	tRWD	130			
tWLCL	Delay time, W low to CAS low (early write cycle)	twcs	- 5	- 5		กร
^t GHD	Delay time, \overline{G} high before data applied at DQ		3D	40		ns
t _{rf}	Refresh time interval	tREF	4		4	ms

Note: All cycle times assume t_t = 5 ns.

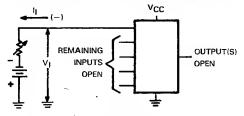
Page mode only.

^{***} Necessary to insure G has disabled the output buffers prior to applying data to the device.

[†] In a read-modify-write cycle, tCLWL and tsu(WCH) must be observed. Depending on the user's transition times, this may require additional CAS low time tw(CL).

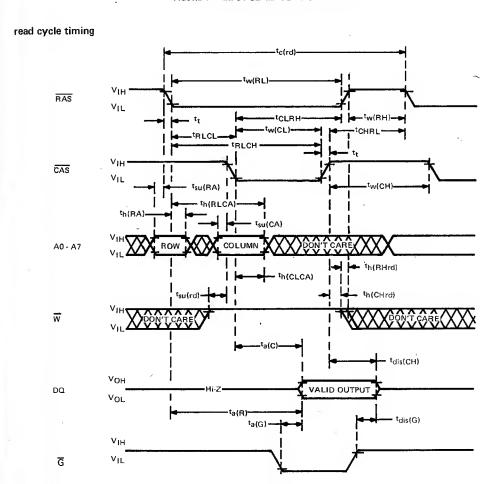
[‡] In a read-modify-write cycle, t_{RLWL} and t_{su(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time tw(RL)

PARAMETER MEASUREMENT INFORMATION

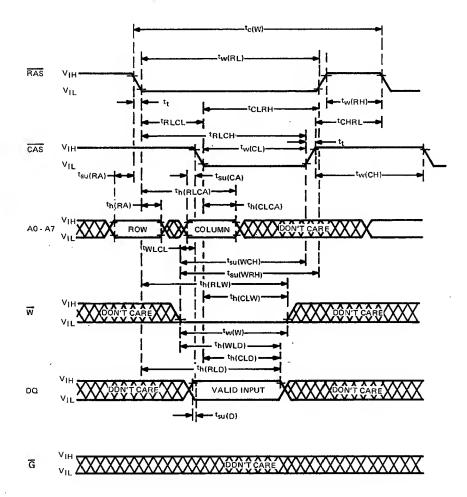


NOTE: Each input is tested separately.

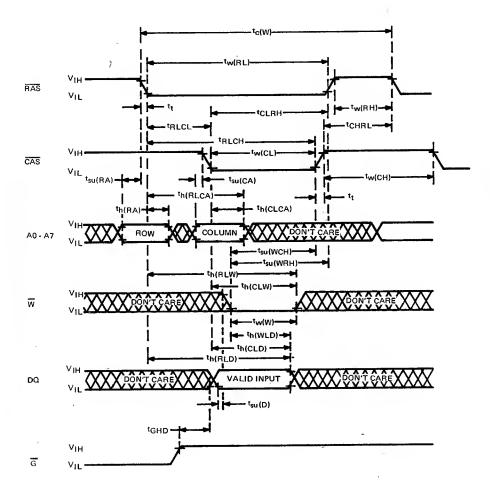
FIGURE 1 - INPUT CLAMP VOLTAGE TEST CIRCUIT



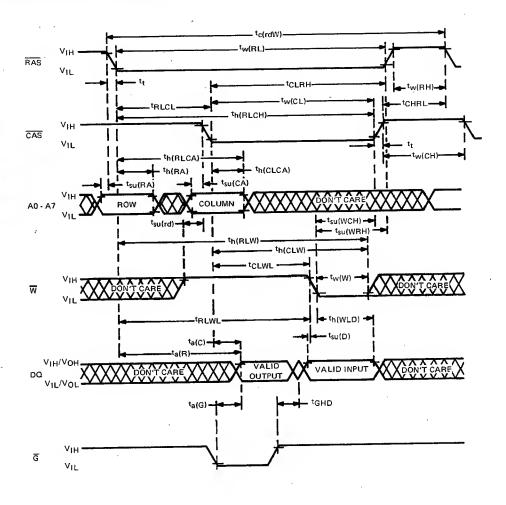
early write cycle timing



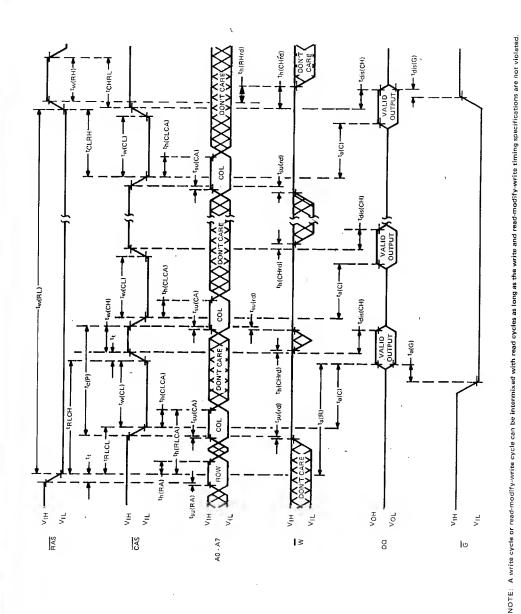
write cycle timing



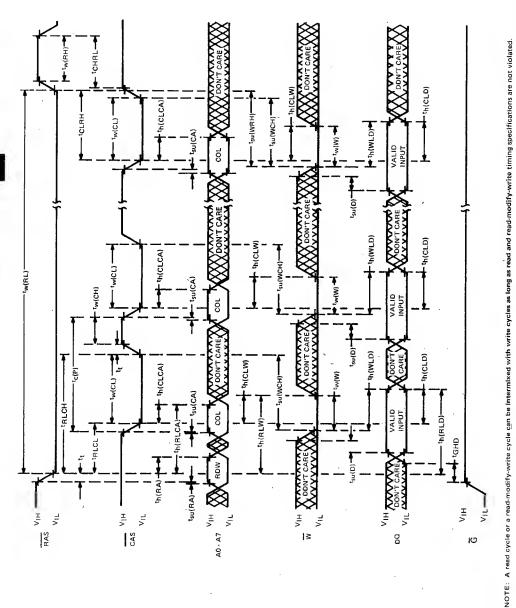
read-write/read-modify-write cycle timing



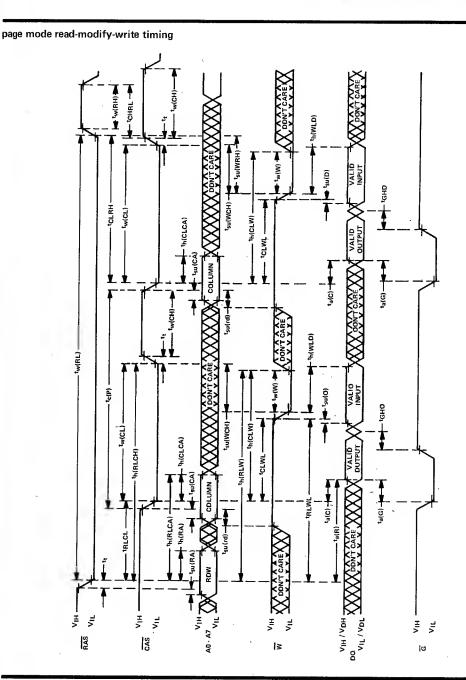
page-mode read cycle timing



page-mode write cycle timing



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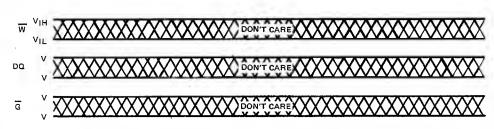


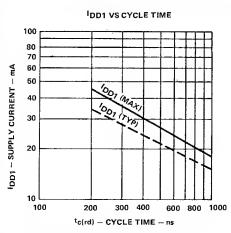
NOTE: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as read and write timing specifications are not violated.

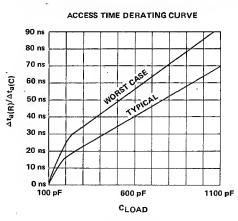
A0 - A7

RAS-only refresh timing | total | tot

ROW







Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.